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09/944,085	09/04/2001	Kazutaka Inukai	12732-073001	3800

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EXAMINER

SHAPIRO, LEONID

ART UNIT	PAPER NUMBER
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2673

DATE MAILED: 01/15/2004

8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/944,085

Applicant(s)

KAZUTAKA ET AL.

Examiner

Leonid Shapiro

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 November 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-45 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-45 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings were received on 11-25-03. These drawings are Figs. 10A-10B.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1, 5, 9, 13, 17, 21, are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Newly introduced limitation: "wherein a bit number of a first display period among the $n+m$ display periods is different from a bit number of a last display period among the $n+m$ display periods" is not supported in specification. On Page 14, Lines 4-5 only have the description of display periods $Tr1$ to Trn and on Page 18, Lines 18-21 only have the description, that the divided display periods corresponding to the same bit of the digital video signal do not appear in succession. There is no description in specification related to the first and last display periods among the $n+m$ display periods.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3, 5-7,9-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Someya (US Patent No. 6,040,819) in view of Kane (US Patent No. 6,229,508 B1) and Naka et al. (US Patent No. 6,518,977 B1).

As to claim 1, as best understood by examiner, Someya teaches a method of driving an EL display device including a plurality of pixels, the method comprising: dividing a frame period into $n + m$ display periods (with n and m being natural numbers) of one or more, wherein the $n + m$ display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, a plurality of display periods, among the $n + m$ display periods correspond to the same bit of the digital video signal, and other display periods corresponding to other bits of the digital video signal, among the $n + m$ display periods, appear between the plurality of display periods (See Fig. 6, items SF9-1, SF8-SF1 and SF9-2, in description See Col. 34, Lines 47-57).

Someya does not show first, second and third TFT and an organic EL element, for each of the $n + m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off.

Kane teaches first (N1), second (N3) and third (N2) TFT and an organic EL element (See Fig. 5, items N1-N3, 550, in description See Col. 5, Lines 56-59), inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49); and after each of the $n + m$ display periods begins, completing the respective display period by beginning another display period or by turning on the third TFT (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49); wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the three TFTs driving method as shown by Kane in the Someya apparatus and method in order to implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

Someya and Kane do not show a bit number of a first display period among the $n+m$ display periods is different from a bit number of a last display period among the $n+m$ display periods.

Naka et al. teaches a bit number of a first display period is different from a bit number of a last display period (See Fig. 19, items SF0, SF8, in description See Col. 13, Lines 33-47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement different bit numbers for the first and the last periods as shown by Naka et al. in the

Someya and Kane apparatus and method in order to make the light periodicity more random and reduce false contour interference (See Col. 12, Lines 23-26 in the Naka et al. reference).

As to claim 5, Someya teaches a method of driving an EL display device including a plurality of pixels, the method comprising: dividing a frame period into $n + m$ display periods (with n and m being natural numbers) of one or more, wherein the $n + m$ display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, a plurality of display periods, among the $n + m$ display periods correspond to the most significant bit of the digital video signal, and other display periods corresponding to other bits of the digital video signal, among the $n + m$ display periods, appear between the plurality of display periods (See Fig. 6, items SF9-1, SF8-SF1 and SF9-2, in description See Col. 34, Lines 47-57).

Someya does not show first, second and third TFT and an organic EL element, for each of the $n + m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT; and after each of the $n + m$ display periods begins, completing the respective display period by beginning another display period or by turning on the third TFT; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off.

Kane teaches first (N1), second (N3) and third (N2) TFT and an organic EL element (See Fig. 5, items N1-N3, 550, in description See Col. 5, Lines 56-59), inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49); and after each of the $n + m$ display periods begins, completing the respective display period by beginning

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another display period or by turning on the third TFT (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49); wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the three TFTs driving method as shown by Kane in the Someya apparatus and method in order to implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

Someya and Kane do not show a bit number of a first display period among the $n+m$ display periods is different from a bit number of a last display period among the $n+m$ display periods.

Naka et al. teaches a bit number of a first display period is different from a bit number of a last display period (See Fig. 19, items SF0, SF8, in description See Col. 13, Lines 33-47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement different bit numbers for the first and the last periods as shown by Naka et al. in the Someya and Kane apparatus and method in order to make the light periodicity more random and reduce false contour interference (See Col. 12, Lines 23-26 in the Naka et al. reference).

As to claim 9, Someya teaches a method of driving an EL display device including a plurality of pixels, the method comprising: dividing a frame period into $n + m$ display periods (with n and m being natural numbers) one or more, wherein the $n + m$ display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, upper bits of the digital video signal correspond to a plurality of display periods among the $n + m$ display

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periods, and other display periods corresponding to other bits of the digital video signal, among the $n + m$ display periods, appear between the plurality of display periods (See Fig. 6, items SF9-1, SF8-SF1 and SF9-2, in description See Col. 34, Lines 47-57).

Someya does not show first, second and third TFT and an organic EL element, for each of the $n + m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off.

Kane teaches first (N1), second (N3) and third (N2) TFT and an organic EL element (See Fig. 5, items N1-N3, 550, in description See Col. 5, Lines 56-59), inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49); and after each of the $n + m$ display periods begins, completing the respective display period by beginning another display period or by turning on the third TFT (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49); wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the three TFTs driving method as shown by Kane in the Someya apparatus and method in order to implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

Someya and Kane do not show a bit number of a first display period among the $n+m$ display periods is different from a bit number of a last display period among the $n+m$ display periods.

Naka et al. teaches a bit number of a first display period is different from a bit number of a last display period (See Fig. 19, items SF0, SF8, in description See Col. 13, Lines 33-47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement different bit numbers for the first and the last periods as shown by Naka et al. in the Someya and Kane apparatus and method in order to make the light periodicity more random and reduce false contour interference (See Col. 12, Lines 23-26 in the Naka et al. reference).

As to claim 13, Someya teaches a method of driving an EL display device including a plurality of pixels, the method comprising: dividing a frame period into $n + m$ display periods (with n and m being natural numbers) of one or more, wherein the $n + m$ display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, a plurality of display periods, among the $n + m$ display periods correspond to the same bit of the digital video signal, and other display periods corresponding to other bits of the digital video signal, among the $n + m$ display periods, appear between the plurality of display periods (See Fig. 6, items SF9-1, SF8-SF1 and SF9-2, in description See Col. 34, Lines 47-57).

Someya does not show first, second TFT and an organic EL element, for each of the $n+m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off.

Kane teaches first (N1), second (N2) and an organic EL element (See Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53), for each of the $n + m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT; and after each of the $n + m$ display periods begins, completing the respective display period by beginning another display period; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off (See Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the two TFTs driving method as shown by Kane in the Someya apparatus and method in order to implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

Someya and Kane do not show a bit number of a first display period among the $n + m$ display periods is different from a bit number of a last display period among the $n + m$ display periods.

Naka et al. teaches a bit number of a first display period is different from a bit number of a last display period (See Fig. 19, items SF0, SF8, in description See Col. 13, Lines 33-47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement different bit numbers for the first and the last periods as shown by Naka et al. in the Someya and Kane apparatus and method in order to make the light periodicity more random and reduce false contour interference (See Col. 12, Lines 23-26 in the Naka et al. reference).

As to claim 17, Someya teaches a method of driving an EL display device including a plurality of pixels, the method comprising: dividing a frame period into $n + m$ display periods

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(with n and m being natural numbers) of one or more, wherein the $n + m$ display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, a plurality of display periods, among the $n + m$ display periods correspond to the most significant bit of the digital video signal, and other display periods corresponding to other bits of the digital video signal, among the $n + m$ display periods, appear between the plurality of display periods (See Fig. 6, items SF9-1, SF8-SF1 and SF9-2, in description See Col. 34, Lines 47-57).

Someya does not show first, second TFT and an organic EL element, for each of the $n + m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off.

Kane teaches first (N1), second (N2) and an organic EL element (See Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53), for each of the $n + m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT; and after each of the $n + m$ display periods begins, completing the respective display period by beginning another display period; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off (See Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the two TFTs driving method as shown by Kane in the Someya apparatus and method in order to implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

Someya and Kane do not show a bit number of a first display period among the $n+m$ display periods is different from a bit number of a last display period among the $n+m$ display periods.

Naka et al. teaches a bit number of a first display period is different from a bit number of a last display period (See Fig. 19, items SF0, SF8, in description See Col. 13, Lines 33-47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement different bit numbers for the first and the last periods as shown by Naka et al. in the Someya and Kane apparatus and method in order to make the light periodicity more random and reduce false contour interference (See Col. 12, Lines 23-26 in the Naka et al. reference).

As to claim 21, Someya teaches a method of driving an EL display device including a plurality of pixels, the method comprising: dividing a frame period into $n + m$ display periods (with n and m being natural numbers) of one or more, wherein the $n + m$ display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, upper bits of the digital video signal correspond to a plurality of display periods among the $n + m$ display periods, and other display periods corresponding to other bits of the digital video signal, among the $n + m$ display periods, appear between the plurality of display periods (See Fig. 6, items SF9-1, SF8-SF1 and SF9-2, in description See Col. 34, Lines 47-57).

Someya does not show first, second TFT and an organic EL element, for each of the $n+m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off.

Kane teaches first (N1), second (N2) and an organic EL element (See Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53), for each of the $n + m$ display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT; and after each of the $n + m$ display periods begins, completing the respective display period by beginning another display period; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off (See Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the two TFTs driving method as shown by Kane in the Someya apparatus and method in order to implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

Someya and Kane do not show a bit number of a first display period among the $n+m$ display periods is different from a bit number of a last display period among the $n+m$ display periods.

Naka et al. teaches a bit number of a first display period is different from a bit number of a last display period (See Fig. 19, items SF0, SF8, in description See Col. 13, Lines 33-47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement different bit numbers for the first and the last periods as shown by Naka et al. in the Someya and Kane apparatus and method in order to make the light periodicity more random and reduce false contour interference (See Col. 12, Lines 23-26 in the Naka et al. reference).

As to claims 2,6,10,14,18 and 22, Kane teaches the first and second TFT have the same polarity (See Fig. 2, items N1-N2 and Fig. 5, items N1, N3).

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As to claims 3,7,11,15,19 and 23, Someya teaches $Tr_1, Tr_2, Tr_3, \dots Tr_{n-1} = 2^0, 2^1, 2^2, \dots, 2^{n-2}, 2^n$, where the lengths of the display periods, among the $n-m$ display periods, corresponding to respective bits of the digital video signal are taken as $Tr_1, Tr_2, Tr_3, \dots Tr_{n-1}, Tr_n$ (Fig.9, items SF1-SF8, in description See Col. 1, Lines 10-35).

As to claims 12,16 and 20, Kane teaches the first TFT function as a switching TFT and the second TFT function as an EL driver TFT (See Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53).

As to claims 25,27,29,31-33, Someya teaches after each of the $n+m$ display periods begins, the respective display periods are completed by beginning of another display period (See Fig. 6, items SF9-1, SF8-SF1 and SF9-2, in description See Col. 34, Lines 47-57).

As to claims 26,28,30, Kane teaches after each $n+m$ display periods begins, the respective display completed by third TFT turning on (See Fig. 5, items N2-N3,AZ, in description See Col. 6, Lines 12-18).

As to claims 34,36,38,40,42,44 Someya teaches the first display period is a divided display period in one frame period (See Fig. 6, item SF9-1) and Naka et al. teaches the last display period is a display period in one frame period (See Fig. 19, item SF8).

As to claims 35,37,39,41,43,45 Naka et al. teaches the first display period is one of the plurality of display periods in frame period and the last display period is one of the other display periods in frame period (See Fig. 19, items SF0, SF8).

5. Claims 4, 8 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Someya, Kane and Naka et al. as aforementioned in claims 1, 5 and 9 in view of Kanatani et al. (US Patent No. 4,070,663).

Kane teaches the first TFT function as a switching TFT (See Fig. 5, item 530, in description See Col. 5, Line 59-60), the second TFT function as an EL driver TFT (See Fig. 5, item 510, in description See Col. 5, Line 59-60), and third TFT function as a TFT, connected to Autozero line (See Fig. 5, item 520, in description See Col. 5, Line 61-62).

Someya, Kane and Naka et al. do not show third TFT connected to the erase line.

Kanatani et al. teaches erasing data line (See Fig. 25, item j, in description See Col. 19, Lines 37-54).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace Autozero line with erase line as shown by Kanatani et al. in the Someya, Kane and Naka et al. apparatus and method in to implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

Response to Amendment

6. Applicant's arguments filed on 11-25-03 with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9314.

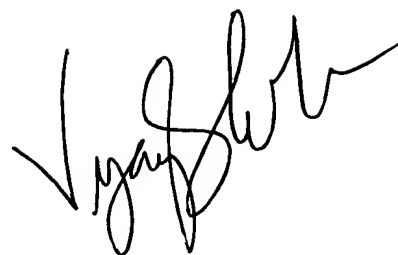
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

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A handwritten signature in black ink, appearing to read 'Vijay Shankar', written in a cursive style.

VIJAY SHANKAR
PRIMARY EXAMINER